AF 2133

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 09/882,417
Filed: June 15, 2001
Inventor(s):
Chambers et al.

Title: A Circuit and Method For Correcting Erroneous Data In Memory For Pipelined Reads

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Examiner: Abraham, Esaw T.
Group/Art Unit: 2133
Atty. Dkt. No: 5500-67700

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Stephen J. Curran
Printed Name

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4/20/05
Date

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal of March 2, 2005, Appellant presents this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

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I. REAL PARTY IN INTEREST

The subject application is owned by Advanced Micro Devices, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at One AMD Place, Sunnyvale, California 94088, as evidenced by the assignment recorded at Reel 011914, Frame 0605.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-15 are pending in the present application. Claims 1-15 stand finally rejected and are the subject of this appeal. A clean copy of claims 1-15, as on appeal (incorporating all amendments), is included in the Appendix hereto.

IV. STATUS OF AMENDMEMNTS

No amendment to the claims has been filed subsequent to the final rejection. The Appendix hereto reflects the current state of the rejected claims.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

"A computer system may employ error correcting code (ECC) circuits which allow the system to detect and/or correct erroneous data. The ECC circuits may be used in various capacities by the system. In some systems, a memory controller may employ an ECC circuit to correct errors in data returned from the system memory. A separate ECC circuit may be used in the processor." (*See* Specification page 1)

"Many memory controllers include the ECC circuit in the data path to and from main memory. In such memory controllers, the ECC circuit may generate an error correction code for data written to memory. As read requests arrive, a memory request queue and associated command logic processes the read requests by placing the read request onto a command bus. When that data is returned from memory, the ECC circuit may use the corresponding error correction code to detect an error in the data. Many ECC circuits also correct the error on the fly and since the ECC circuit is in the data path, the corrected data may be sent to the requesting device. This method is common and may provide a relatively fast data return time, especially for pipelined reads. However, the erroneous data is left in memory." (Emphasis added) (*See* Specification page 1)

"To correct the erroneous data stored in memory, another type of memory controller may be used. In such a memory controller, a read buffer may be employed which stores the address and data returned from each read request. The ECC circuit may first correct the data and then store the corrected version in the buffer. Alternatively, the erroneous data may be stored in the buffer and corrected at a later time. In the former case, once any pending read requests are processed, the corrected data corresponding to each read request may be subsequently written back into memory into the respective memory locations. In the latter case, the erroneous data may be read out of the buffer and the ECC circuit may correct the data. The corrected data corresponding to each read request may be subsequently written back into memory into the respective memory location." (Emphasis added) (*See* Specification pages 1 and 2)

"Thus in this type of memory controller, the erroneous data in memory may be replaced by a corrected version. Replacing erroneous data with a corrected version is sometimes referred to as scrubbing. However, as described above, a buffer may be used that is large enough to hold the entire data path. As data bus widths increase, the size of such a buffer may become necessarily large. In addition, other factors such as latencies associated with the data arrival and read wait states may also necessitate a large buffer. A

corresponding increase in the area required to manufacture the die may also be necessary. Since there is a direct relationship between die area and manufacturing costs, it may be desirable to have a memory controller that provides memory data scrubbing without the use of a buffer which stores the data returned from a read request." (Emphasis added) (*See* Specification pages 1 and 2)

"In one embodiment, a memory controller includes a control unit, a storage unit and an error detection and correction unit. The control unit is coupled to the storage unit and configured to read data including an associated error correction code from a memory subsystem in response to a memory read request. The storage unit may be any type of storage such as a register bank, for example. The error detection and correction unit is coupled to receive the data and configured to determine whether an error exists in that data based upon the associated error correction code. The control unit is configured to store an indication in the storage unit that the data corresponding to the memory read request is erroneous. The control unit is further configured to **detect the indication** in the storage unit and to responsively perform a subsequent read of the data from the memory subsystem and to **write a corrected version of the data back to the memory subsystem**." (Emphasis added) (*See* Specification page 3)

"In one particular implementation, the error detection and correction unit is configured to provide the corrected version of the data **in response to the subsequent read** of the data. In another implementation, the indication includes an address in the memory subsystem of the erroneous data corresponding to the read request." (Emphasis added) (*See* Specification page 3)

The specification also discloses at page 7, lines 1-12 "...storage unit 130 of FIG. 2 may be configured to store an indication, including an address, that data associated with a read request has an error. Storage unit 130 may also be configured to detect the indication and to generate a read request of the erroneous data and to generate a write request of a corrected version of the data to main memory subsystem 30 of FIG. 1.

Control unit 110 may be configured to handle memory transaction requests from processor 10, graphics adapter 40 of FIG. 1 and peripheral bus controller 70 of FIG. 2. As will be described in greater detail below, control unit 110 may also be configured to accept the read request from storage unit 130 and to perform the subsequent read of the erroneous data in response to the read request and to write the corrected version of the data to main memory subsystem 30 of FIG. 1." (Emphasis added) (*See* Specification page 3)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-15 are rejected under 35 U.S.C. § 103(a) as being patentable over Gonzales et al (U.S. Patent Number 6,101,614) (hereinafter "Gonzales").

VII. ARGUMENT

A. Claims 1-15

The Examiner rejected claims 1-15 as being obvious over Gonzales under 35 U.S.C. § 103(a). Appellant respectfully traverses this rejection in light of the following remarks.

The Examiner asserted in the Final Office Action dated December 3, 2004, the "Applicant argues that the prior art of record (Gonzales et al.) do not teach a control unit configured to detect in storage unit and to perform a read data from memory." The Examiner went on to disagree and assert "applicant's concedes on column 3 last paragraph and abstract that Gonzales teach a method and apparatus for automatically scrubbing ECC errors in memory upon detecting correctable errors in data read from a memory through the use of write back path coupled between the outputs of the read and write data buffers of a memory controller." The Examiner then maintained the prior art rejection based on this assumption.

Appellant respectfully disagrees with the Examiner's assertions and his characterization of Gonzales. Specifically, Appellant, in fact, did not argue as the Examiner has suggested. More particularly, Appellant argued (as below) that Gonzales does not teach or suggest "responsively perform a subsequent read of said data from said memory subsystem" as recited in Appellant's claim 1.

In addition, in response to the Examiner's allegation that Appellant conceded anything. Appellant merely quoted from column 3 of Gonzales (as below) to illustrate what Gonzales actually discloses. Appellant did not agree or concede to anything. To the contrary, (as below) Appellant argued that it appeared that Gonzales merely discloses a system including features similar to the system disclosed in Appellant's APA.

Appellant's claim 1 recites, in pertinent part,

> "a control unit configured to read data including an associated error correction code from a memory subsystem in response to a memory read request;...
> an error detection and correction unit coupled to receive said data and configured to determine whether an error exists in said data based upon said associated error correction code;
> wherein said control unit is configured to store **an indication** in said storage unit **that said data corresponding to said memory read** request **is erroneous**; and
> wherein said control unit is further configured to subsequently detect said indication in said storage unit and to **responsively perform a subsequent read of said data from said memory subsystem** and to **write a corrected version of said data within said memory subsystem**." (Emphasis added)

Gonzales, at column 3, lines 1-34, discloses "Data read from memory is checked for errors and stored in the data read buffer. If the memory controller detects a correctable ECC error in the read data, it corrects the data **as it is being written into the read buffer**... the memory control logic issues a memory scrub command... to signal that **the corrected data within the read buffer is to be written back** to the memory location from which it came... the selected control source then asserts a read strobe to the read data buffer to read the data out of the buffer... the corrected data is written to the location in memory specified by the original read request." (Emphasis added)

On page 4, of the Office Action dated March 17, 2004, the Examiner acknowledged Gonzales stores the erroneous data by stating "Gonzales et al. is basically identifying or indicating an error and configuring to store an erroneous data."

From the foregoing, Gonzales teaches a system similar to that described in the AAPA [*see background page 1, line 27 through page 2 line 6*]. As such, Gonzales teaches retaining the **corrected data** within **a read buffer** that is separate from main memory, then writing that corrected data back to memory. This method of writing corrected data back to memory clearly teaches away from the Appellant's invention.

More particularly, as described in the Appellants' background section of the Specification, Appellant's invention seeks to provide corrected data back to memory without the use of a read data buffer. Appellant submits Gonzales does not perform a subsequent read of the erroneous data from memory. Instead, Gonzales stores corrected data in the read buffer, gains control of the writeback path and reads the corrected data from the read buffer and writes that corrected data back to memory. This is clearly different than Appellant's claimed invention.

Accordingly, Appellant submits Gonzales **neither teaches nor suggests** "responsively perform **a subsequent read of said data from said memory subsystem**

and to write a corrected version of said data within said memory subsystem" as recited in Appellant's claim 1.

Appellant further highlights claim 2, which recites "wherein said error detection and correction unit is further configured to provide said corrected version of said data **in response to said subsequent read** of said data." Appellant submits this feature is clearly **not taught nor fairly suggested** by Gonzales.

Thus, Appellant believes claim 1, along with its dependent claims, to patentably distinguish over Gonzales for the reasons given above.

Appellant's claims 6 and 11 recite features that are similar to the features recited in claim 1. Therefore, Appellant believes claims 6 and 11, along with their respective dependent claims, to patentably distinguish over Gonzales for at least the reasons given above with respect to claim 1.

VII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-15 was erroneous, and reversal of his decision is respectfully requested.

Respectfully submitted,

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Date: April 20, 2005

IX. APPENDIX

The claims on appeal are as follows.

1. A memory controller comprising:

a control unit configured to read data including an associated error correction code from a memory subsystem in response to a memory read request;

a storage unit coupled to said control unit;

an error detection and correction unit coupled to receive said data and configured to determine whether an error exists in said data based upon said associated error correction code;

wherein said control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and

wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from said memory subsystem and to write a corrected version of said data within said memory subsystem.

2. The memory controller as recited in claim 1, wherein said error detection and correction unit is further configured to provide said corrected version of said data in response to said subsequent read of said data.

3. The memory controller as recited in claim 1, wherein said indication includes an address in said memory subsystem of said data corresponding to said read request.

4. The memory controller as recited in claim 1, wherein said control unit is further configured to inhibit accepting an additional memory read request in response to said indication.

5. The memory controller as recited in claim 4, wherein said control unit is further configured to accept said additional memory read request in response to said subsequent read of said data from said memory subsystem and a corrected version of said data being written to said memory subsystem.

6. A data processing system comprising:

a processor;

a memory subsystem configured to store data;

a system controller including a memory controller coupled between said processor and said memory subsystem, wherein said memory controller includes:

a control unit configured to read data including an associated error correction code from a memory subsystem in response to a memory read request;

a storage unit coupled to said control unit;

an error detection and correction unit coupled to receive said data and configured to determine whether an error exists in said data based upon said associated error correction code;

wherein said control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and

wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from said memory subsystem and to write a corrected version of said data within said memory subsystem.

7. The data processing system as recited in claim 6, wherein said error detection and correction unit is further configured to provide said corrected version of said data in response to said subsequent read of said data.

8. The data processing system as recited in claim 6, wherein said indication includes an address in said memory subsystem of said data corresponding to said read request.

9. The data processing system as recited in claim 6, wherein said control unit is further configured to inhibit accepting an additional memory read request in response to said indication.

10. The data processing system as recited in claim 9, wherein said control unit is further configured to accept said additional memory read request in response to said subsequent read of said data from said memory subsystem and a corrected version of said data being written to said memory subsystem.

11. A method of correcting erroneous data in a memory of a memory subsystem, said method comprising:

reading data including an associated error correction code from said memory subsystem in response to a memory read request;

receiving said data and determining whether an error exists in said data based upon said associated error correction code;

storing an indication that said data corresponding to said memory read request is erroneous; and

subsequently detecting said indication and responsively performing a subsequent read of said data from said memory subsystem and writing a corrected version of said data within said memory subsystem.

12. The method as recited in claim 11 further comprising providing said corrected version of said data in response to said subsequent read of said data.

13. The method as recited in claim 11, wherein said indication includes an address in said memory subsystem of said erroneous data corresponding to said read request.

14. The method as recited in claim 11 further comprising inhibiting accepting an additional memory read request in response to said indication.

15. The method as recited in claim 14 further comprising accepting said additional memory read request in response to performing said subsequent read of said data from said memory subsystem and to said writing of said corrected version of said data to said memory subsystem.

X. EVIDENCE APPENDIX

No evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

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Stephen J. Curran
Printed Name

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April 20, 2005
Date

2

FEE AUTHORIZATION

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The Commissioner is hereby authorized to charge the following fee to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5500-67700:

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Respectfully submitted,

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